National Semiconductor

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SCAN12100
1228.8 and 614.4 Mbps CPRI SerDes with Auto RE Sync and Precision Delay Calibration Measurement

General Description

The SCAN12100 is a 1228.8 and 614.4 Mbps serializer/deseralizer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. The SCAN12100 integrates precision delay calibration measurement (DCM) circuitry that measures link delay components to better than ± 800 ps accuracy.

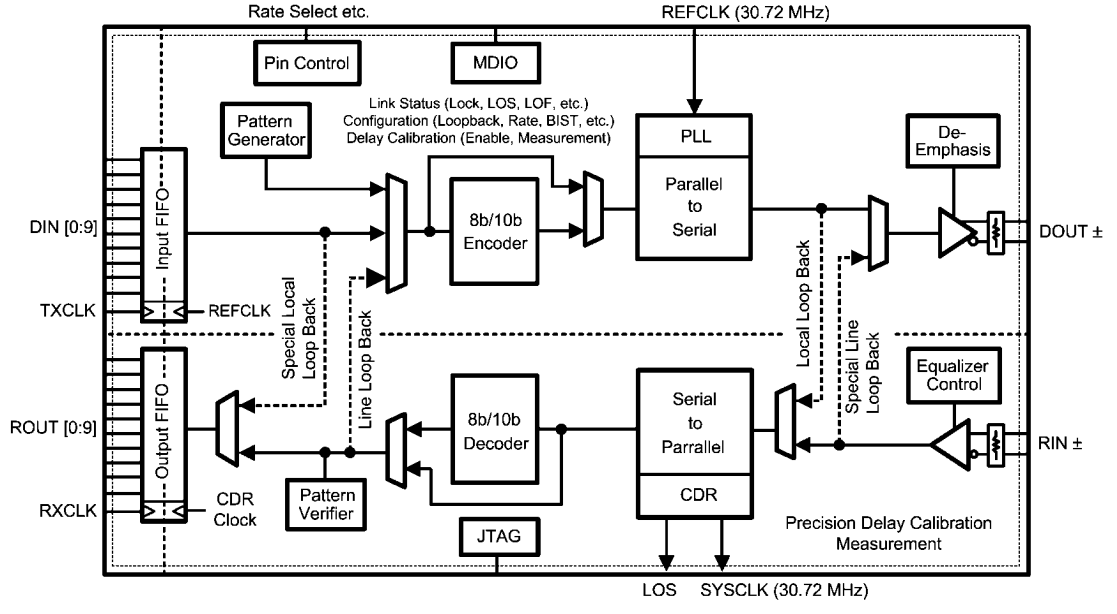
The SCAN12100 features independent transmit and receive PLLs, on-chip oscillator, and intelligent clock management circuitry to automatically perform remote radio head synchronization and reduce the cost and complexity of external clock networks.

The SCAN12100 is programmable though an MDIO interface as well as through pins, featuring configurable transmitter de-emphasis, receiver equalization, speed rate selection, internal pattern generation/verification, and loop back modes. In addition to at-speed BIST, the SCAN12100 includes IEEE 1149.1 and 1149.6 testability.

Features

- Exceeds LV and HV CPRI voltage and jitter requirements
- 1228.8, and 614.4 Mbps operation
- Pin and package compatibility with the SCAN25100
- Integrated delay calibration measurement (DCM) directly measures T14 and Toffset delays to ≤ ± 800 ps
- DCM also measures chip and other delays to ≤ ± 1200 ps accuracy
- Deterministic chip latency
- Independent transmit and receive PLLs for seamless RE synchronization
- Low noise recovered clock output
- Requires no jitter cleaning in single-hop applications
- >8 kV ESD on the CML IO, >7 kV on all other pins, >2 kV CDM
- Hot plug protection
- LOS, LOF, 8b/10b line code violation, comma, and receiver PLL lock reporting
- Programmable hyperframe length and start of hyperframe character
- Programmable transmit de-emphasis and receive equalization with on-chip termination
- Advanced testability features
  - IEEE 1149.1 and 1149.6
  - At-speed BIST pattern generator/verifier
  - Multiple loopback modes
- 1.8V or 3.3V compatible parallel bus interface
- 100-pin TQFP package with exposed dap
- Industrial –40 to +85° C temperature range

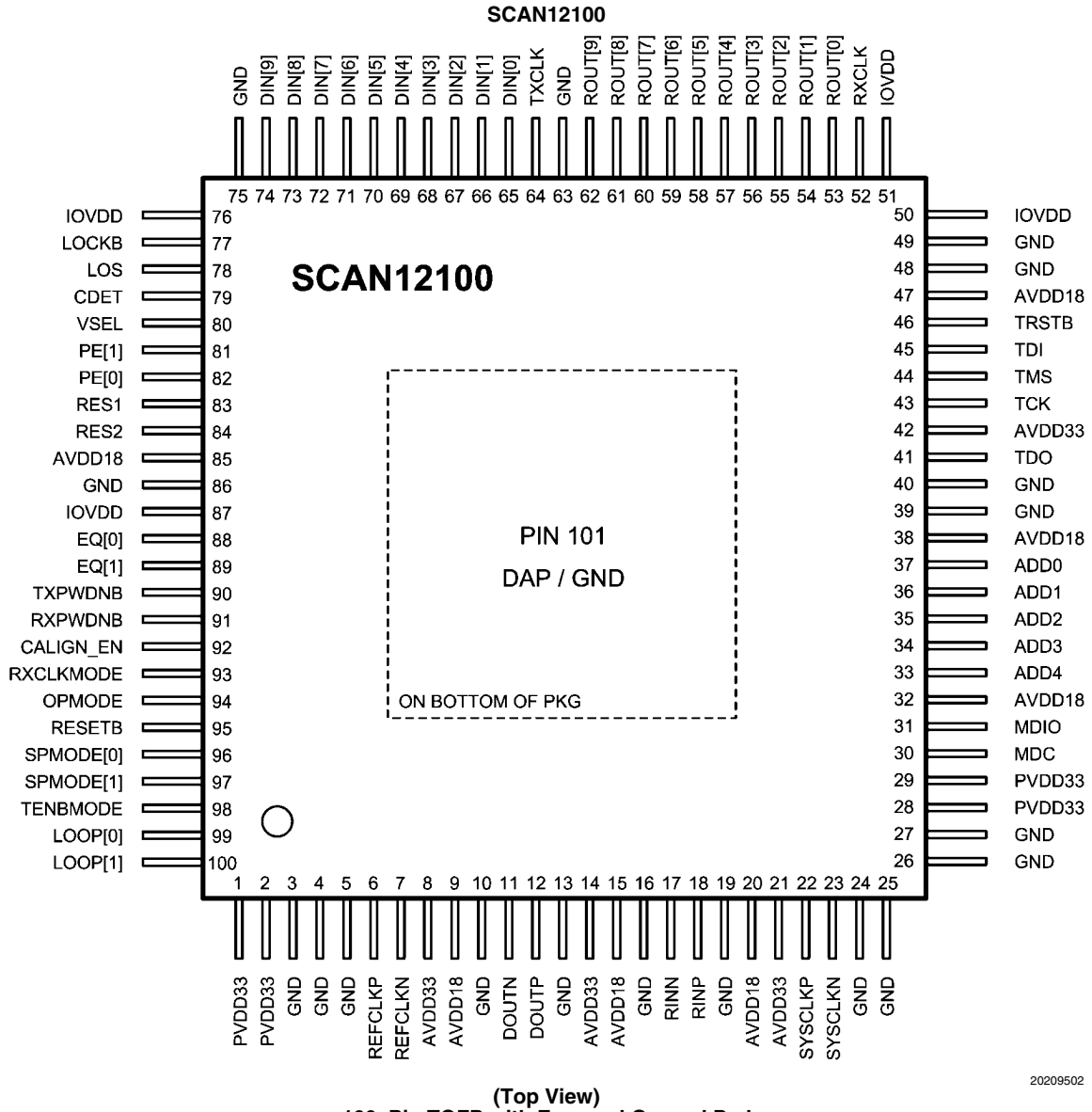
Block Diagram



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Pin Diagram



(Top View)
100–Pin TQFP with Exposed Ground Pad
Order Number SCAN12100TYA
See NS Number VXF100B

Pin Descriptions

Pin #	Pin Name	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
12 11	DOUTP DOUTN	O, CML	Inverting and non-inverting high speed CML differential outputs of the serializer. On-chip termination resistors connect from DO+ and DO– to an internal reference
18 17	RINP RINN	I, CML	Inverting and non-inverting high speed differential inputs of the deseralizer. On-chip termination resistors connect from RI+ and RI– to an internal reference. On-chip termination resistors are configured for AC-coupled applications.
PARALLEL DATA BUS			
65 66 67 68 69 70 71 72 73 74	DIN [0] DIN [1] DIN [2] DIN [3] DIN [4] DIN [5] DIN [6] DIN [7] DIN [8] DIN [9]	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmit data word. In 10-bit mode, the 10-bit code-group at DIN [0–9] is serialized with the internal 8b/10b encoder disabled. Bit 9 is the msb. In 8-bit mode, DIN [0-7] is first converted into 10-bit code-group by the internal 8b/10b encoder before it is serialized. Bit 7 is the msb. DIN [8] is used as K-code select pin and DIN[9] should be tied Low. When DIN [8] is low, DIN [0-7] is mapped to the corresponding 10-bit D-group. When DIN [8] is high, DIN [0-7] is mapped to the corresponding 10-bit K-group. The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2
53 54 55 56 57 58 59 60 61 62	ROUT [0] ROUT [1] ROUT [2] ROUT [3] ROUT [4] ROUT [5] ROUT [6] ROUT [7] ROUT [8] ROUT [9]	O, LVTTL or 1.8V LVCMOS Internal pull down	Deserialized receive data word. In 10-bit mode, ROUT [0-9] is the deserialized received data word in 10-bit code group. Bit 9 is the msb. In 8-bit mode, ROUT [0-7] is the deserialized received data byte. Bit 7 is the msb. ROUT [8] is the K-group indicator. A low at ROUT [8] indicates ROUT [0-7] belongs to the D-group, while a high indicates it belongs to the K-group. ROUT [9] is the line code violation (LCV) indicator. ROUT [9] is high for one ROUT cycle when a line code violation occurs. The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2
CLOCK SIGNALS			
6 7	REFCLKP REFCLKN	I, LVDS or LVPECL	Inverting and non-inverting differential serializer reference clock. A low jitter clock source should be connected to REFCLKP & REFCLKN.
64	TXCLK	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmit clock. TXCLK must be synchronous to REFCLK to avoid FIFO under/overflow though it may differ in phase.
52	RXCLK	I/O, LVTTL or 1.8V LVCMOS	Write mode: RXCLK is recovered clock output pin. Read mode: RXCLK is an input pin. ROUT [9:0] are latched out on RXCLK rising and falling edges. RXCLK must be synchronous to the incoming serial data to avoid FIFO over/underflow, though it may differ in phase. See RXCLKMODE pin description for more details.
22 23	SYSCLKP SYSCLKN	O, LVDS	30.72 MHz output clock. (OPMODE must be low.)
LINE STATUS			
78	LOS	O, LVTTL or 1.8V LVCMOS	Receiver CPRI loss of signal (LOS) status (8-bit mode only). 0 = signal detected (per CPRI standard) 1 = signal lost (per CPRI standard) See “LOS Detection” under “Functional Description” for more details.
77	LOCKB	O, LVTTL or 1.8V LVCMOS	Receiver PLL lock status 0 = Receiver PLL locked 1 = Receiver PLL not locked

Pin #	Pin Name	I/O, Type	Description
79	CDET	O, LVTTL or 1.8V LVCMOS	Comma Detect. 0 = no comma yet detected in the incoming serial stream or receiver PLL not locked. 1 = the receiver PLL is locked and a positive or negative comma bit sequence detected in the incoming bit stream. The serial to parallel converter is aligned to the proper 10-bit word boundary when comma alignment is enabled (CALIGN_EN = 1).
CONTROL PINS			
82 81	PE [0] PE [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Transmitter de-emphasis configuration. Pulling both pins low enables MDIO control, default is no de-emphasis.
			PE1 / **PE0** /
			0 / 0 / No de-emphasis
			0 / 1 / Low de-emphasis
			1 / 0 / Medium de-emphasis
			1 / 1 / Maximum de-emphasis
88 89	EQ [0] EQ [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Receive input equalization configuration. Pulling both pins low enables MDIO control, default is no receive equalization.
			EQ1 / **EQ0** /
			0 / 0 / No receive equalization
			0 / 1 / Low receive equalization
			1 / 0 / Medium receive equalization
			1 / 1 / Maximum receive equalization
90 91	TXPWDNB RXPWDNB	I, LVTTL or 1.8V LVCMOS Internal pull down	Power down control signals. **TXPWDNB** 0 = Transmitter is powered down and DOUT± pins are high impedance. 1 = Transmitter is powered up. **RXPWDNB** 0 = Receiver is powered down and ROUT [9:0] as well as LOS, LOCKB, CDET, RXCLK, and SYSCLK are high impedance. 1 = Receiver is powered up.
92	CALIGN_EN	I, LVTTL or 1.8V LVCMOS Internal pull down	Comma alignment enable. 0 = comma alignment circuitry disabled. Receiver will not realign 10-bit data based on incoming comma characters. CDET pin still flags comma detection. 1 = comma detect and alignment circuitry enabled. Receiver aligns 10-bit data to incoming comma character and flags comma detect through CDET pin.
93	RXCLKMODE	I, LVTTL or 1.8V LVCMOS Internal pull down	Receiver recovered clock mode 0 = Write mode. RXCLK pin is a recovered clock output. (RXCLK = output pin) 1 = Read mode. RXCLK pin is ROUT [9:0] bus read input strobe. (RXCLK = input pin)
80	VSEL	I, LVTTL or 1.8V LVCMOS Internal pull down	Selects whether single-ended data and control pins are 3.3V LVTTL or 1.8V LVCMOS. 0 = 1.8V LVCMOS. Tie VSEL to ground and power IOVDD at 1.8 V. 1 = 3.3V LVTTL. Tie VSEL to IOVDD supply and power IOVDD at 3.3 V.
94	OPMODE	I, LVTTL or 1.8V LVCMOS Internal pull down	Selects SerDes mode. 0 = Base station mode 1 = Reserved for future use
95	RESETB	I, LVTTL or 1.8V LVCMOS Internal pull down	Hardware SerDes reset. Resets PLLs and MDIO registers. 0 = Hardware SerDes reset 1 = Normal operation

Pin #	Pin Name	I/O, Type	Description
96 97	SPMODE [0] SPMODE [1]	I, LVTTL or 1.8V LVCMOS Internal pull down	Speed mode configuration. (OPMODE must be low) Pulling both pins low enables MDIO control.

SPMODE [1]	SPMODE [0]	
0	0	Rate selected via MDIO
0	1	614.4 Mbps rate mode
1	0	1228.8 Mbps rate mode
1	1	Reserved

98	TENBMODE	I, LVTTL or 1.8V LVCMOS, Internal pull down	Enable 10-bit mode The 8B/10B specification is defined in IEEE 802.3-2000 section 36.2.2 0 = Selects 8-bit mode. Enables the internal 8b/10b encoder and decoder. 1 = Selects 10-bit mode. Bypasses internal 8b/10b encoder and decoder.
99 100	LOOP [0] LOOP [1]	I, LVTTL or 1.8V LVCMOS, Internal pull down	Loop back configuration. Pulling both pins low enables MDIO control. Note: During Special line (remote) loop back mode, the output de-emphasis control is disabled.

LOOP [1]	LOOP [0]	
0	0	Normal mode—no loop back
0	1	Line (remote) loop back mode
1	0	Local loop back mode
1	1	Special line (remote) loop back mode

MDC/MDIO			
30 31 37 36 35 34 33	MDC MDIO ADD0 ADD1 ADD2 ADD3 ADD4	3.3V LVTTL Internal pull up on ADDR pins	MDC/MDIO configuration bus. Protocol per IEEE 802.2ae-2002 MDC/MDIO Clause 45. These pins are 3.3V LVTTL compatible, not 1.2V signal compatible.
IEEE 1149.1 (JTAG)			
45 41 44 43 46	TDI TDO TMS TCK TRSTB	3.3V LVTTL Internal pull up on TDI, TMS, and TRSTB	JTAG test bus for IEEE 1149.1 and 1149.6 support.
RESERVED PINS			
83 84	RES1 RES2	I	Reserved. Tie with 5 KΩ resistor to ground.
POWER			
9, 15, 20, 32, 38, 47, 85	AVDD18	I, Power	1.8V analog supply.
8, 14, 21, 42	AVDD33	I, Power	3.3V analog supply.
1, 2, 28, 29	PVDD33	I, Power	3.3V PLL supply (minimize supply noise to < 100 mV peak-to-peak).
50, 51, 76, 87	IOVDD	I, Power	1.8V or 3.3V parallel I/O bus and control pin supply. See VSEL pin description for additional information.
GROUND			
3, 4, 5, 10, 13, 16, 19, 24, 25, 26, 27, 39, 40, 48, 49, 63, 75, 86	GND	I, Ground	Device ground.

Pin #	Pin Name	I/O, Type	Description
GROUND DAP			
101	GND	I, Ground	Device ground. Pad must be soldered and contected to GND plane with a minimum of 8 thermal vias to achieve specified thermal performance.

Note: I= input O = output Internal pull down = input pin is pulled low by an internal resistor Internal pull up = input pin is pulled high by an internal resistor

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (AV_{DD18})	−0.3V to +2.0V
Supply Voltage (PV_{DD}, IOV_{DD})	−0.3V to +3.6V
Supply Voltage (AV_{DD33})	−0.3V to +3.6V
LVCMOS Input Voltage	−0.3V to (IOV_{DD} + 0.5V)
LVCMOS Output Voltage	−0.3V to (IOV_{DD} + 0.5V)
MDC/MDIO/ADD[0:4],VSEL Input Voltage	−0.3V to (AV_{DD33} + 0.5V)
MDIO Output Voltage	−0.3V to (AV_{DD33} + 0.5V)
CML Receiver Input Voltage	−0.3V to (AV_{DD} + 0.3V)
CML Receiver Output Voltage	−0.3V to (AV_{DD} + 0.3V)
Junction Temperature	+125°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
Soldering, 10–20 sec	235 °C
Lead-free +260°C flow is available	
Maximum Package Power Dissipation at 25°C	
100-pin TQFP with Exposed Pad	4.16 W
Derating above 25°C	41.6 mW/°C
Thermal Resistance , θ_{JA} (0 airflow)	24.0°C/W
ESD Rating	
CML RIN/DOUT Pins	
HBM, 1.5 kΩ, 100 pF	>8 kV
EIAJ, 0Ω, 200 pF	>250V
CDM	>2 kV
All Other Pins	
HBM, 1.5 kΩ, 100 pF	>7 kV
EIAJ, 0Ω, 200 pF	>250V
CDM	>2 kV

Note: This is the maximum TQFP-100 package power dissipation capability. For SCAN12100 power dissipation, see the information in the Electrical Characteristics section.

Recommended Operating Conditions

	Min	Typ	Max	Unit
Supply Voltage				
AV_{DD18}	1.7	1.8	1.9	V
AV_{DD33}, PV_{DD33}	3.135	3.3	3.465	V
IOV_{DD} (1.8V Mode)	1.7	1.8	1.9	V
IOV_{DD} (3.3V Mode)	3.135	3.3	3.465	V
Temperature	-40	25	85	°C
Junction temperature			125	°C
Supply Noise (Peak-to-Peak)			<100	mV

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
LVCMOS DC SPECIFICATIONS (1.8V I/O)						
V_{IH}	High level input voltage		$0.65V_{DD}$			V
V_{IL}	Low level input voltage				$0.35V_{DD}$	V
I_{IN}	Input Current	V_{IN} = 0V or 1.9V	−10		+50	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	1.2			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.45	V
I_{OZ}	Power Down Output Current	Power down	−20		+20	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
LVCMOS DC SPECIFICATIONS (3.3V I/O)						
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.465V	−10		+50	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
I_{OZ}	Power Down Output Current	Power down	−20		+20	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
JTAG DC SPECIFICATIONS (3.3V I/O)						
V_{IH}	High level input voltage		2			V
V_{IL}	Low level input voltage				0.8	V
I_{IN}	Input Current	V_{IN} = 0V or 3.465V	−35		+50	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
MDIO/MDC/ADD0-4 DC SPECIFICATIONS						
V_{IH}	High level input voltage		2.0		3.465	V
V_{IL}	Low level input voltage		GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 or 3.465V	-150		+150	µA
V_{OH}	High level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2 mA			0.4	V
I_{OZ}	Power Down Output Current	Power down	−100		+100	µA
C_{IO}	Input/Output Capacitance	Typical		2.8		pF
POWER CONSUMPTION						
P_D	Max total power consumption	614.4 Mbps				
		Parallel I/O at 1.9V		920	1040	mW
		Parallel I/O at 3.465V		1040	1150	mW
	PRWS pattern embedded in hyperframe Output loading: CML: AC-coupled CMOS: 50Ω transmission line	1228.8 Mbps				
		Parallel I/O at 1.9V		950	1100	mW
		Parallel I/O at 3.465V		1110	1250	mW
POWER CONSUMPTION (Powerdown)						
P_{PDN}	Powerdown Mode	Rx and Tx Powerdown		25	40	mW
TYPICAL POWER CONSUMPTION (By Supply)						
P_{DS}	PVDD33	1228.8 Mbps operation Parallel I/O at 3.3V PRWS pattern embedded in hyperframe		285		mW
	AVDD33			160		mW
	IOVDD			230		mW
	AVDD18			435		mW
RECOMMENDED REFCLK INPUT SPECIFICATIONS						
$V_{IDSREFCLK}$	Differential input voltage		± 100			mV_{P-P}
V_{ICM}	Common mode voltage		0.05V		2.4V	V
f_{REF}	REFCLK frequency	OPMODE = 0 (BTS SerDes Mode)	30	30.72	31.5	MHz
df_{REF}	REFCLK frequency variation	Variation from nominal frequency	−100		+100	ppm
t_{REF-DC}	REFCLK duty cycle	Between 50% of the differential voltage across REFCLKP and REFCLKN	45		55	%
t_{REF-X}	REFCLK transition time	Transition time between 20% and 80% of the differential voltage across REFCLKP and REFCLKN		300		pS
SYSCLK DC OUTPUT SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	± 250	± 330	± 450	mV
V_{OS}	Offset Voltage		1.125	1.20	1.375	V
I_{OS}	Output Short Circuit Current	Output pair shorted together and tied to GND			35	mA
I_{OZ}	Power Down Output Current	Power down	−30		+30	µA
TRANSMITTER SERIAL TIMING SPECIFICATIONS						
V_{OD}	Output differential voltage swing	PE[1]=0, PE[0]=0	± 550	± 700	± 800	mVp-p
		PE[1]=0, PE[0]=1		± 630		mVp-p
		PE[1]=1, PE[0]=0		± 500		mVp-p
		PE[1]=1, PE[0]=1	± 200	± 360	± 450	mVp-p
R_{DO}	Output differential resistance		80	100	120	Ω

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
R_O	Output Return Loss	Frequency = 1.229 GHz		-13.4		dB
t_R, t_F	Serial data output transition time (Notes 11, 15)	Measured between 20% and 80%	80	100	130	ps
JIT_{T-DJ}	Serial data output deterministic jitter (Notes 3, 11)	Output CJPAT with BER of 10^{-12} (Note 4)			0.14	UIp-p
JIT_{T-TJ}	Serial data output total jitter (Notes 3, 11)	Output CJPAT pattern with BER of 10^{-12} (Note 4)			0.279	UIp-p
$t_{LAT-ACC-T}$	Transmit latency variation at start up (Notes 11, 6, 8)	614.4 Mbps			36	ns
		1.228 Gbps			18	
t_{LAT-T}	Transmit latency (Note 8)	614.4 Mbps		310		ns
		1.228 Gbps		155		
$t_{DO-LOCK}$	Maximum lock time	K28.5 pattern at 1228.8 Mbps		110	130	us
RECEIVER SERIAL TIMING SPECIFICATIONS						
V_{ID}	Input voltage	RINP - RINN	± 100		± 1100	mVp-p
V_{CMR}	Receiver common mode voltage			0.9		V
R_R	Differential Input Terminations		80	100	120	Ω
RLR_I	Input Return Loss (Note 11)	Frequency = 1.229 GHz		-20	-15	dB
t_{LAT-R}	Receive latency (Note 9)	614.4 Mbps		280		ns
		1.228 Gbps		140		ns
t_{LAT-R}	Receive latency variation at start up (Notes 11, 6, 9)	614.4 Mbps			36	ns
		1.228 Gbps			18	ns
JIT_{R-TOL}	Total input jitter tolerance (Note 11)	Input CJPAT with BER of 10^{-12} (Note 4)			0.66	UIp-p
F_{R-LOCK}	Receiver lock range	Input data rate reference to local transmit data rate.	–200		+200	ppm
t_{R-LOCK}	Maximum lock time	K28.5 pattern at 1228.8 Mbps			1	ms
TRANSMITTER INPUT TIMING SPECIFICATIONS						
t_{S-T}	Setup Time	DIN [9:0] valid to TXCLK rising or falling edge	0.5			ns
t_{H-T}	Hold Time	TXCLK rising or falling edge to DIN [9:0] valid	0.5			ns
t_{DC}	Duty cycle	TXCLK duty cycle	45		55	%
f_{TXCLK}	TXCLK frequency		30		62.5	MHz
RECEIVER OUTPUT TIMING SPECIFICATIONS (Read Mode RXCLKMODE=1)						
t_{PDRX}	RXCLK Propagation Delay	RXCLK rising or falling edge to ROUT [9:0] valid	2	4	6	ns
t_{DC}	Duty cycle	RXCLK input duty cycle	45		55	%
f_{RXCLKR}	RXCLK input frequency	RXCLK input frequency	30		62.5	MHz
t_R, t_F	Output data transition time	For ROUT [0-9], LOCK, etc. pins. Measured between 20% and 80% levels		0.35		ns
RECEIVER OUTPUT TIMING SPECIFICATIONS (Write Mode RXCLKMODE=0)						
t_{S-R}	Setup Time	ROUT [9:0] valid to RXCLK rising or falling edge (Note 10)	2.2			ns
t_{H-R}	Hold Time	RXCLK rising or falling edge to ROUT [9:0] valid (Note 10)	2.4			ns
t_{DC}	Duty cycle	RXCLK duty cycle	45		55	%
f_{RXCLK}	RXCLK frequency		30		62.5	MHz

Symbol	Parameter	Condition	Min	Typ (Note 2)	Max	Units
t_R, t_F	Output data transition time	For ROUT [0-9], LOCK, etc. pins. Measured between 20% and 80% levels		0.35		ns
CDET OUTPUT TIMING SPECIFICATIONS (Read Mode RXCLKMODE=1)						
t_{PDCD}	CDET Propagation Delay	RXCLK rising or falling edge to CDET	2	4	6	ns
CDET OUTPUT TIMING SPECIFICATIONS (Write Mode RXCLKMODE=0) (Note 5)						
t_{S-C}	Setup Time	CDET valid to RXCLK rising or falling edge	2.6			ns
t_{H-C}	Hold Time	RXCLK rising or falling edge to CDET valid	2.6			ns
SYSCLK LVDS OUTPUT TIMING SPECIFICATIONS						
$t_{SYSCLKNDC}$	Duty cycle		40		60	%
JIT_{SYSCLK}	Cycle to cycle jitter	(Note 11)		40	65	ps p-p
t_R, t_F	Output transition time	Between 20% and 80% levels (Note 11)	0.1		0.3	ns
MDC/MDIO TIMING SPECIFICATIONS (Clause 45)						
f_{MDC}	MDC Frequency		0		2.5	MHz
t_{S-MDIO}	Setup Time	MDIO (input) valid to MDC rising clock	10			ns
t_{H-MDIO}	Hold Time	MDC rising edge to MDIO (input) invalid	10			ns
t_{D-MDIO}	Delay Time	MDIO (output) delay from MDC rising edge	0		300	ns
t_{X-MDIO}	Transition Time	Measured at MDIO when used as output, CL = 470 pF		1		ns
MINIMUM PULSE WIDTH, Hardware Reset (Note 12)						
t_{TX-RST}	Transmiter Reset	TXPWDNB = 0		1		us
t_{RX-RST}	Receiver Reset	RXPWDNB = 0		1		us
t_{RST}	SerDes Reset	RESETB = 0		1		us
JTAG TIMING SPECIFICATIONS						
f_{JTAG}	JTAG TCK Frequency	R_L= 1000Ω, C_L = 15 pF	25			MHz
t_{R-J} t_{F-J}	TDO data transition time (20% to 80%)			2		ns
t_{S-TDI}	Setup Time TDI to TCK High or Low		2			ns
t_{H-TDI}	Hold Time TDI to TCK High or Low		2			ns
t_{S-TMS}	Setup Time TMS to TCK High or Low		2			ns
t_{H-TMS}	Hold Time TMS to TCK High or Low		2			ns
t_{W-TCK}	TCK Pulse Width		10			ns
t_{W-TRST}	TRSTB Pulse Width		2.5			ns
t_{REC}	Recovery Time TRSTB to TCK		14			ns
DELAY CALIBRATION MEASUREMENT (DCM) (Notes 11, 13, 14)						
T_{14}	T_{14} Delay Accuracy	Receive and Transmit PLLs locked to valid hyperframe data.			± 800	ps
T_{offset}	T_{offset} Delay Accuracy				± 800	ps
T_{ser}	Serializer Delay Accuracy				± 1200	ps
T_{des}	Deserializer Delay Accuracy				± 1200	ps
T_{in-out}	T_{in-out} Delay Accuracy				± 1200	ps
T_{out-in}	T_{out-in} Delay Accuracy				± 1200	ps

Note 1: “Absolute Maximum Ratings” are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

Note 2: Typical parameters are measured at nominal supply levels and T_A = 25°C. They are for reference purposes and are not production-tested.

Note 3: Transmit Jitter testing methodology is defined in Appendix 48B of IEEE 802.2ae-2002. The SCAN12100 transmit output jitter is constant for all valid CPRI datarates. The transmit jitter is significantly less than the specified limits in terms of UI.

Note 4: CJPAT is a stress pattern defined in IEEE 802.2ae-2002 Appendix 48A

Note 5: CDET nominal valid duration is determined by the CPRI data rate. CDET timing is similar to the ROUT[0:9] timing.

Note 6: Transmit or Receive K28.5 pattern. Assumes TXCLK is stable and toggles only after all SerDes clocks become synchronous.

Note 7: Conditions: The TX PLL is locked, the TXCLK is stable and the TXCLK is synchronous.

Note 8: Transmit latency is fixed once the link is established and is guaranteed by the Tser specification.

Note 9: Receive latency is fixed once the link is established and is guaranteed by the Tdes specification.

Note 10: Receiver output timing specifications for TS-R and TH-R are tested at the CPRI rate of 1.2288 Gbps.

Note 11: Limits are guaranteed by design and characterization over process, supply voltage, and temperature variations.

Note 12: Limits are guaranteed by design.

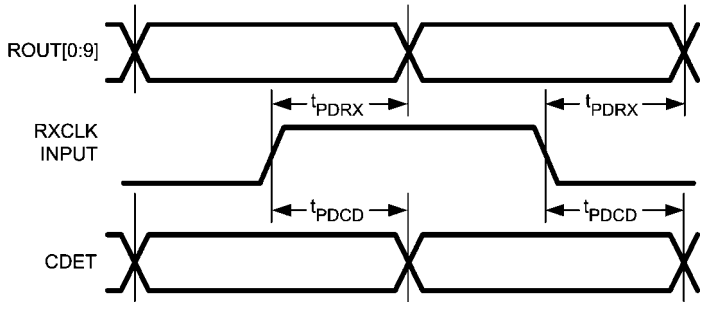
Note 13: Serial side DCM readings are referenced to the first bit of the K28.5 pattern {110000 0101 001111 1010}. Parallel side DCM readings are referenced to the TXCLK or RXCLK edge (not the data edge) that registers the K character as an input or output.

Note 14: DCM readings are valid when the RXCLK pin on the SCAN12100 is used as an output in "WRITE" mode (RXCLKMODE = 0) and IOVDD = 3.3V.

Note 15: Edge rate characterization includes the loading effects of 1.0 uF AC-coupling capacitors and 4 inches of 100 ohm differential microstrip.

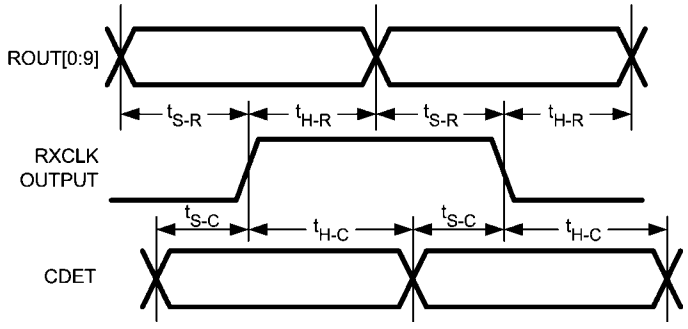
AC Timing Diagrams

READ MODE



20209509

WRITE MODE



20209510

Functional Description

POWER UP AND LINK SYNCHRONIZATION

An internal power on reset (POR) circuit disables the transmitter output and sets receiver ROUT[9:0], LOS, LOCKB, and CDET in static high state for approximately 150 ms (150ms is based on an internal counter monitoring the 30.72 MHz REFCLK) to allow external clock sources to stabilize. A special power up sequence is not required. Once the transmitter powers up and TXCLK becomes active, the transmitter starts sending valid data. Once the receiver is powered up and REFCLK exists, the receiver is ready to receive data. When comma alignment is enabled (CALIGN_EN = 1), the receiver searches for a valid comma in the incoming stream. When a comma is detected, the receiver performs code group (comma) alignment and presents data on ROUT.

To ensure the parallel bus FIFO read/write pointer distance is half of the total FIFO depth, the following procedure should be followed (e.g., after reset or comma (re)alignment):

1. Power up SCAN12100 while holding TXCLK and RXCLK (in read mode) input clocks static low or high. The SCAN12100 will hold both transmitter and receiver FIFO's in reset until the TXCLK and RXCLK start toggling.
2. Wait for all clock sources to become synchronous and stable based on the CPRI timing specification.
3. Toggle TXCLK and RXCLK input clocks to latch data into and out of the parallel DIN/ROUT buses.
4. If at any time the clock requires a resynchronization, such as switching 30.72 MHz system clock. Holding TXCLK and RXCLK (in read mode) static high or low resets the SCAN12100 internal FIFO pointers.

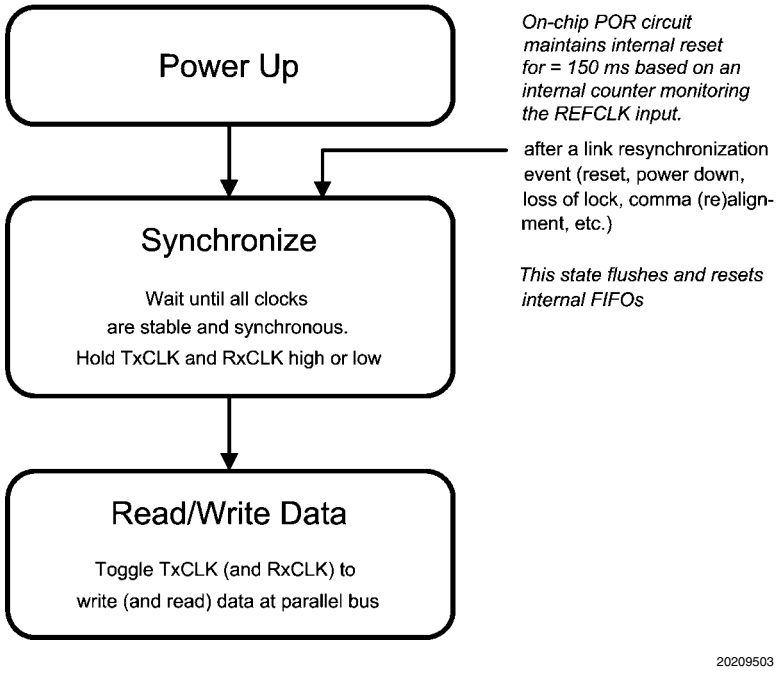


FIGURE 1. Power up State Diagram

POWER DOWN

When the transmitter is powered down by pulling pin TXPWDNB down, DOUT is put into a high impedance state. When the receiver is powered down by pulling RXPWDNB down, ROUT[9:0], LOS, LOCKB, CDET, RXCLK, and SYSCLK are high impedance. The MDC/MDIO signal pins are not powered down when TXPWDNB and/or RXPWDNB are low.

Resetting the SCAN12100

The SCAN12100 has a rich set of hardware and software reset functions. When performing hardware pin resets, TXPWDNB and RXPWDNB pins or the RESETB pin must be held low for at least 1 us.

TABLE 1. Reset Conditions

Reset Type	What is Reset
Initial power up	All internal states and registers held at reset for 150 ms after power on. This reset period is based on an internal counter monitoring the 30.72 MHz REFCLK input signal.
TXPWDNB and RXPWDNB low for ≥ 1 us	All internal states and registers are reset
RESETB low for ≥ 1 us	Logic reset (including MDIO)
Write “0” to MDIO RESETB register	Logic reset (excluding MDIO)
SPMODE change	Logic reset (excluding MDIO)
TXCLK missing for ≥ 7 cycles	Transmit FIFO flushed, transmit read/write pointers reset
RXCLK missing for ≥ 7 cycles (Read Mode)	Receive FIFO flushed, receive read/write pointers reset
TRSTB (IEEE 1149.1 interface)	Only IEEE 1149.1 state machine is reset

Deterministic FIFO Delay at Start Up

To ensure synchronous operation, REFCLK, TXCLK, and RXCLK should be stable and the receiver synchronized before data is sent into or out of the parallel buses.

SCAN12100 CLOCK DOMAINS

Most SerDes have only two clocks: a reference clock (that also acts as a transmit clock) and a receive recovered clock. The sharing of clocks in these architectures, however, can cause loss of lock issues during RE synchronization. To provide seamless base station synchronization, the SCAN12100 features independent transmit and receive PLLs and four clock signals.

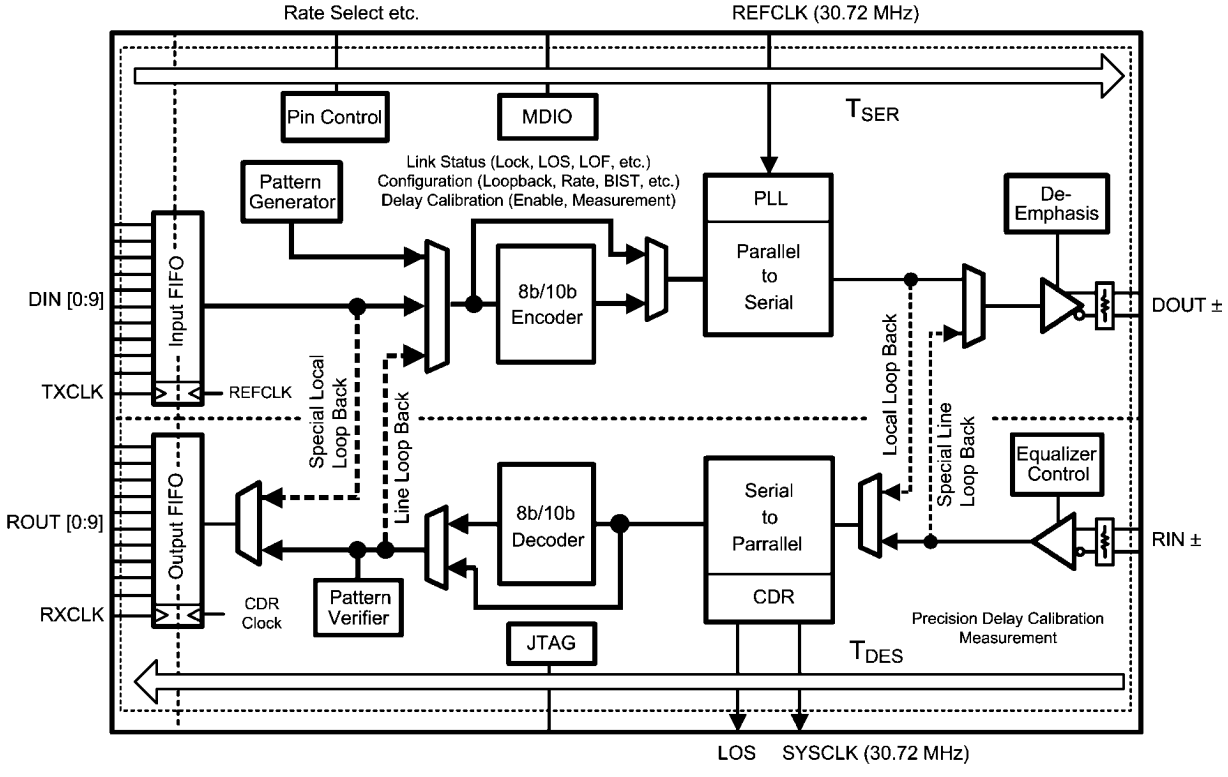


FIGURE 2. SCAN12100 Clock Domains

The SCAN12100 has additional clocking features beneficial for RE applications. The chip’s receiver PLL circuitry is independent of REFCLK and has an integrated oscillator, allowing the receiver to lock to the incoming REC stream and synchronize the RE without losing lock when REFCLK switches from local to recovered clock.

Once the RE is synchronized to the REC, all clocks are synchronous and the four clock domains become one clock domain. Holding TXCLK (and RXCLK if in read mode) static high or static low until the RE is synchronized to the REC ensures the on-chip FIFOs are flushed and reset. Once the system is synchronous, the SCAN12100 chip delays are con-

stant and these and other system delays can be measured using DCM.

SYSCLK AND RXCLK RECOVERED CLOCKS

The SCAN12100 provides two recovered clocks, RXCLK (in write mode) and SYSCLK, with different characteristics:

TABLE 2. Recovered Clock Truth Table

Pin	Type	Before Lock	After Lock	Phase vs. Incoming Serial Stream
RXCLK (write mode)	1.8V CMOS or LVTTL	High-Z	Digital recovered clock synchronous to output data	Can be measured via DCM
SYSCLK	LVDS	30.72 MHz ± 5% (internal oscillator)	30.72 MHz analog recovered clock form deserializer PLL	Not Specified

SYSCLK can be used to synchronize remote radio heads since it provides a local 30.72 MHz internal clock which is gracefully transitioned to the recovered clock. RXCLK is digital and synchronous to recovered output data and its phase versus the incoming serial stream can be precisely measured using DCM. Either or both recovered clocks may be used depending on application requirements.

REFERENCE CLOCK

The differential REFCLKP and REFCLKN input accepts LVDS or LVPECL level signals. For LVDS signals, these pins can be terminated differentially with a 100-Ohm resistor placed across the REFCLKP and REFCLKN inputs.

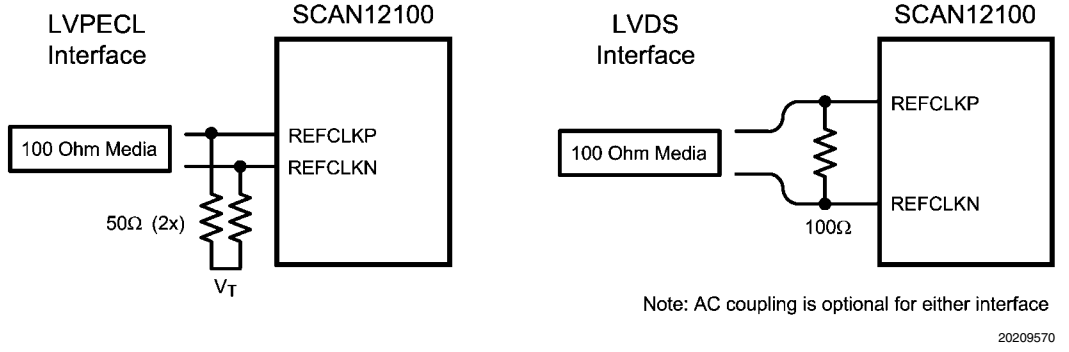


FIGURE 3. SCAN12100 REFCLK Termination

TABLE 3. Reference Clock Input Requirements

REFCLK Mode	Clock Rate	Duty Cycle	Accuracy	Jitter (Typ)	Jitter (Max)
BTS SerDes Mode (OPMODE = 0)	30.72 MHz	40% / 60%	± 100 ppm	40 ps p-p	140 ps p-p

SPMODE[1:0] SPEED RATE SELECTION

The SCAN12100 operates in from a constant 30.72 MHz REFCLK clock and performs necessary clock multiplication internally to support CPRI base station data rates. The speed rate is programmable using the SPMODE[1:0] pins or through MDIO when SPMODE[1:0] are pulled low. MDIO default speed is 1228.8 Mbps on initial power up or reset.

TABLE 4. Speed Rate Configuration Truth Table

OPMODE	SPMODE[1]	SPMODE[0]	REFCLK	TXCLK/RXCLK	Serial Rate
0 (BTS Mode)	0	0	30.72 MHz	MDIO Setting	MDIO Setting
0 (BTS Mode)	0	1	30.72 MHz	30.72 MHz	614.4 Mbps
0 (BTS Mode)	1	0	30.72 MHz	61.44 MHz	1228.8 Mbps
0 (BTS Mode)	1	1	30.72 MHz	Reserved	Reserved

VSEL PIN 1.8CMOS/3.3LVTTL SELECT

The parallel input bus, output bus, and control pins are configurable for either 1.8V CMOS or 3.3V LVTTL compliance. To ensure reliable device operation, the VSEL and IOVDD must be configured properly:

TABLE 5. VSEL Pin Control Options

Compliance	VSEL Control Pin	IOVDD Supply Pins
1.8V CMOS	Tie to ground	1.8V
3.3V LVCMOS	Tie to IOVDD supply (must power up with IOVDD)	3.3V

TRANSMIT DATA

DIN[9:0] Transmit Parallel Input Data

Transmit input data pins DIN[9:0] are latched on both rising and falling edges of TXCLK. By using both TXCLK edges, the clock speed is halved, which reduces high speed design and EMI issues. The transmitter serializes and sends the valid Dx.y or Kx.y code. If an invalid Kx.y code is provided at DIN [9:0], the transmitter sends a K30.7 pattern.

TABLE 6. Transmitter Parallel Input Bus Mapping

Tx Input	10-bit Mode (TENBMODE = 1)	8-bit Mode (TENBMODE = 0)
DIN[0]	Coded Data Bit	Data Bit 0 (A, lsb)
DIN[1]	Coded Data Bit	Data Bit 1 (B)
DIN[2]	Coded Data Bit	Data Bit 2 (C)
DIN[3]	Coded Data Bit	Data Bit 3 (D)
DIN[4]	Coded Data Bit	Data Bit 4 (E)
DIN[5]	Coded Data Bit	Data Bit 5 (F)
DIN[6]	Coded Data Bit	Data Bit 6 (G)
DIN[7]	Coded Data Bit	Data Bit 7 (H, msb)
DIN[8]	Coded Data Bit	D/K Select (Z)
DIN[9]	Coded Data Bit	Pulled low through a 5 kΩ resistor

Transmit Serial Data Output

DOUT is a differential current mode logic (CML) driver. Both DOUTP and DOUTN are terminated with on-chip resistors to an internal bias voltage. The values of the internal termination resistors are controlled to 50Ω ±20%.

Transmitter De-Emphasis

The transmitter serial output provides 3 steps of de-emphasis to compensate for backplanes and cable interconnects. Pulling both PE[1:0] pins low enables MDIO control of de-emphasis.

TABLE 7. Transmit De-emphasis Control Settings

PE[1]	PE[0]	Descriptions
0	0	De-emphasis disabled.
0	1	De-emphasis enabled low (approximately 1 dB).
1	0	De-emphasis enabled medium (approximately 3 dB).
1	1	De-emphasis enabled high (approximately 6 dB).

Transmitter Reset Options

TABLE 8. Transmitter Output Truth Table

TXPWDNB	Tx PLL	DIN[9:0]	Tx FIFO	DOUTP/DOUTN
0	X	x		DOUTP and DOUTN pulled to internal bias
1	Missing REFCLK	x		Undefined
1	Missing TXCLK	x		Logic 1
1	Not Locked	x		DOUTP and DOUTN pulled to internal bias
1	Locked	Valid Dx.y or Kx.y		Normal Serial Data
1	Locked	Invalid Kx.y		K30.7 (8-bit Mode) or Serial Data (10-bit Mode)
1	Locked	x	Underflow / Overflow	K30.7 (8-bit Mode)
1	Not Locked	x	Underflow / Overflow	10'd0 (10-bit Mode)

RECEIVE DATAPATH

Receive Serial Data Input

The receive input (RIN) pins are terminated with on-chip 50Ω ±20% resistors to an internal bias voltage. This bias voltage is set to approximately 1.45 volts above GND. Normally CML signals are AC-coupled and this bias voltage sets the input common mode for the RIN inputs. DC coupling between two SCAN12100 devices is acceptable when required in the application. For other CML outputs AC coupling is required.

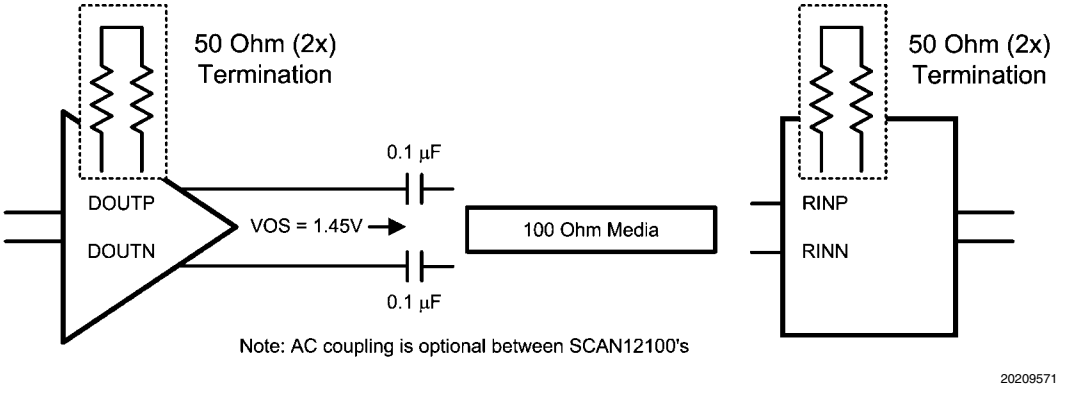


FIGURE 4. SCAN12100 Serial Input Connection

Receive Equalization

The receiver front-end provides 3 steps of equalization filter to compensate for ISI deterministic jitter from lossy backplanes and cables. Pulling both EQ[1:0] pins low enables MDIO control of equalization.

TABLE 9. Receiver Equalizer Control Settings

EQ[1]	EQ[0]	Descriptions
0	0	Equalization disabled.
0	1	Equalization (approximately 2 dB).
1	0	Equalization (approximately 4 dB).
1	1	Equalization (approximately 8 dB).

Receive Output Bus

Receive output data ROUT[9:0] is clocked on both rising and falling edges of RXCLK. By using both RXCLK edges, the clock speed is halved, which reduces EMI issues. The receiver output bus can be configured in either read or write mode.

TABLE 10. Receiver Parallel Output Bus Mapping

Rx Output	10-bit Mode (TENBMODE = 1)	8-bit Mode (TENBMODE = 0)
ROUT[0]	Coded Data Bit	Data Bit 0 (A, lsb)
ROUT[1]	Coded Data Bit	Data Bit 1 (B)
ROUT[2]	Coded Data Bit	Data Bit 2 (C)

Rx Output	10-bit Mode (TENBMODE = 1)	8-bit Mode (TENBMODE = 0)
ROUT[3]	Coded Data Bit	Data Bit 3 (D)
ROUT[4]	Coded Data Bit	Data Bit 4 (E)
ROUT[5]	Coded Data Bit	Data Bit 5 (F)
ROUT[6]	Coded Data Bit	Data Bit 6 (G)
ROUT[7]	Coded Data Bit	Data Bit 7 (H, msb)
ROUT[8]	Coded Data Bit	D/K Flag (Z)
ROUT[9]	Coded Data Bit	Line Code Error Flag

TABLE 11. Receiver Output Truth Table (10-bit Mode, TENBMODE = 1)

RXPWDNB	Rx PLL	RXCLK	SYSCLK	ROUT[9:0]
0	x	High - Z	High - Z	High - Z
1	Missing REFCLK & in 10B mode	High - Z	Undefined	Undefined
1	Not Locked	Based on REFCLK running at DDR Rate	30.72 MHz based on REFCLK	1111111111
1	Locked	Recovered Clock	30.72 MHz based on RXCLK	Deserialized 10-bit Word

WRITE MODE (RXCLKMODE = 0)

In write mode, RXCLK is the recovered clock output. The pins ROUT[9:0], CDET, LOCKB, and LOS are synchronous to RXCLK.

READ MODE (RXCLKMODE = 1)

In read mode, RXCLK is an input and the pins ROUT[9:0], CDET, LOCKB, and LOS are latched by the RXCLK input strobe. Note that for read mode, RXCLK must be synchronous to the incoming serial data stream to avoid receiver FIFO over- and underflow.

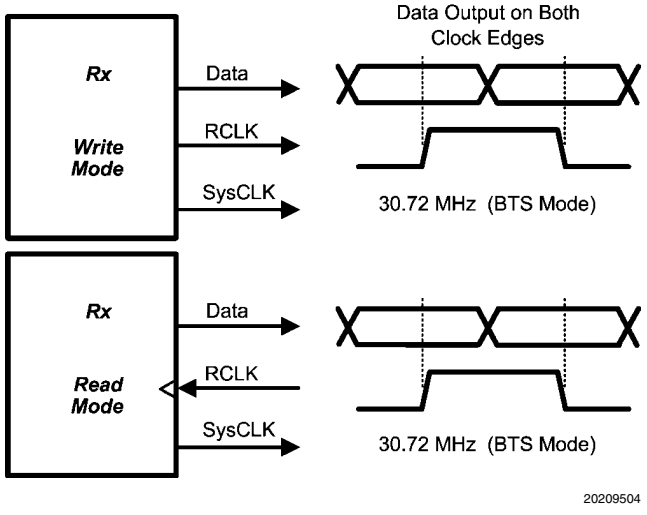


FIGURE 5. Write Mode and Read Mode Diagram

SYSCLK AND RE REMOTE RADIO HEAD SYNCHRONIZATION

The SCAN12100 has independent transmit and receive PLLs as well as an internal ~30.72 MHz oscillator for seamless RE synchronization. Once the SCAN12100 locks to incoming CPRI data, SysCLK becomes phase locked to the recovered clock, automatically synchronizing the RE to the REC. This phase lock transition occurs gracefully through analog circuitry to allow downstream components to track the slight frequency change from external clock to recovered clock. During RE synchronization, TxCLK (and RxCLK if in read mode) should be held static high or low to prevent FIFO over- or under- flow

Unlike most SerDes, the SCAN12100 deserializer does not depend on RefCLK . RefCLK can therefore be switched from a local clock source (crystal oscillator) to the recovered clock without the deserializer losing lock.

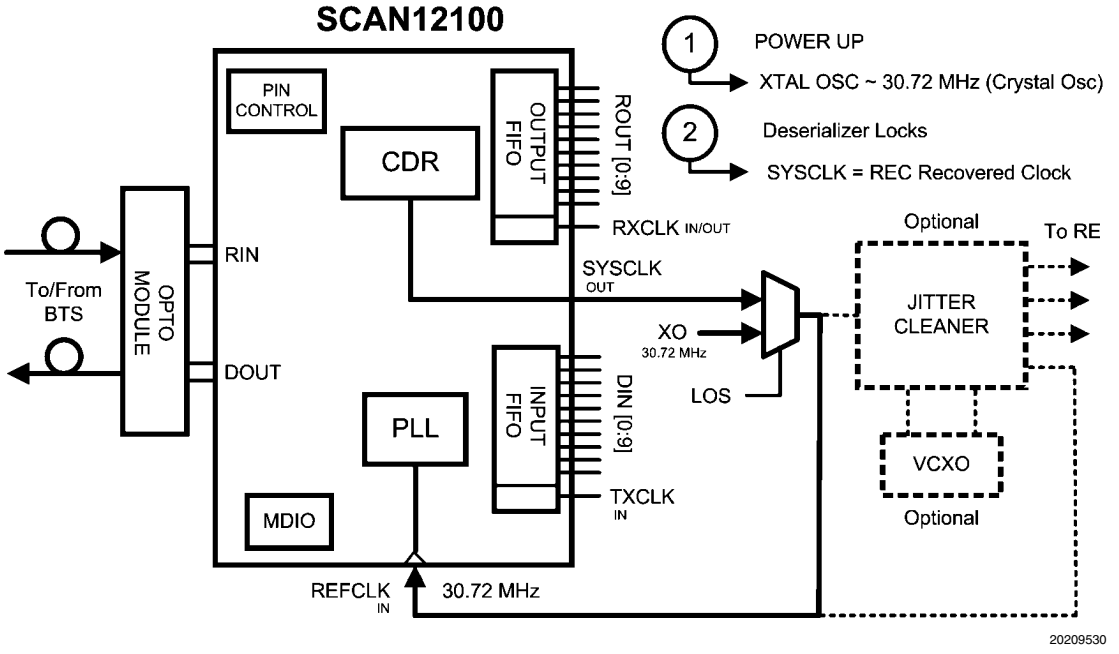


FIGURE 6. Radio Equipment (RE) Clock Syncronization

In multi-hop applications, using a jitter cleaner between SysCLK and RefCLK is recommended to attenuate any accumulated jitter (< 5 MHz).

RECEIVER PLL LOCK DETECTION

The LOCKB pin indicates the lock status of the receive PLL. When asserted high, the receive PLL is not locked to the incoming serial stream. When LOCKB is low, the receive PLL is locked to the incoming serial stream. Line code violations (LCVs) may or may not exist when the PLL is locked.

8B/10B DECODING AND CODE GROUP ALIGNMENT IN 8-BIT MODE

The 8b/10b encodes and decodes all valid Dx.y and Kx.y patterns. These include K23.7, K27.7, K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7, K29.7, and K30.7. The receiver decodes invalid codes to K30.7. K-characters K28.1, K28.5, and K28.7 each contain a comma bit sequence. When comma alignment is enabled (CALIGN_EN = 1), the receiver performs code group alignment when encountering a comma. The CALIGN_EN pin allows the upper layer system to control when alignment and realignment occurs.

COMMA DETECT (CDET) OPERATION

When a K character (K28.1, K28.5, or K28.7) is detected with comma alignment enabled (CALIGN_EN = 1), the receiver performs code group alignment, i.e. the receiver aligns ROUT [9:0] data to the proper word boundary. When the comma is detected, CDET remains high for one 8b/10b word output (RXCLK period/2). When comma alignment is disabled (CALIGN_EN = 0), commas are still detected and flagged at pin CDET, but (re)alignment is not performed.

LOS DETECTION

LOS is set to HIGH during receiver power up, during hardware reset (via RESETB pin), or during software (via RESETB MDIO register) reset. LOS requires one K28.5 character and valid line coding for 1 hyperframe in order to go from HIGH to LOW. After initialization, the LOS is set on the condition shown in the table below. When the deserializer loses lock, LOS is **not** automatically set high since the deserializer continues to count LCV's in order to determine LOS status according to the CPRI standard.

TABLE 12. LOS Set Conditions

OPMODE	Condition	LOS
0 (BTS Mode)	16 or more line code violations in a CPRI hyperframe	1

The LOS mechanism affects the ROUT[9:0] and RXCLK outputs of the device under 8-bit mode. Upon power up, the ROUT[9:0] and RXCLK pins will be static. Once LOS is low, the device will send data on the ROUT[9:0] and RXCLK pins. After LOS is high, the output will continue to send data for 2-3 hyperframes. If there are no line code violations during the next hyperframe, the LOS signal goes low and resumes normal operation. If there are line code violations in the next 2-3 hyperframes, the outputs will be tri-stated and the device enters a reset state.

The LOS function is disabled in 10-bit mode. The LOS defaults high in 10-bit mode.

The LOS signal is reset to low (signal detected) under the following conditions:

TABLE 13. LOS Reset Conditions

OPMODE	Condition	LOS
0 (BTS Mode)	No LCVs occur within a CPRI hyperframe	0

LOF (LOSS OF FRAME) DETECTION

LOF counter is provided through an LOF MDIO status register per CPRI Specification. The LOF function is disabled in 10-bit mode. Under 8-bit mode, LOF will prevent the SCAN12100 DCM scheme from activating. Delay calibration measurement can only be performed when LOF is low.

TEST MODES

Loop Back Modes

The SCAN12100 supports multiple loop back modes for testing device, link, and system operation. The line loop back mode enables the user to check the integrity of the serial data transmission paths. The local loop back verifies operation of the local board. When switching between normal mode and loopback modes, the receiver must synchronize to the new data stream.

Loopback mode can be controlled through the LOOP[1:0] pins or via MDIO. Pulling LOOP[1:0] low enables MDIO control of loopback functions.

TABLE 14. Loopback Control Bit Settings

LOOP[1]	LOOP[0]	Loop Back Mode
0	0	Normal mode—no loop back (enable software program mode)
0	1	Line (remote) loop back mode
1	0	Local loop back mode
1	1	Special line (remote) loop back

At-Speed Built-In Self-Test (BIST)

The SCAN12100 features at-speed built-in self-test (BIST) to support at-speed testing during both manufacturing as well as field diagnosis. Several test patterns are supported including CJPAT lane 0 and PRWS 10.

BIST activation and status are accessed through the Serial Control Interface (MDIO). Multiple registers are used for the control, pattern selection, and customization of the at-speed BIST function. The BIST test results are also reported in BIST status MDIO registers. One-bit BIST_ DETECTED and BIST_PASS status registers are provided to indicate BIST start and pass/fail. A 10-bit counter is used to store the number of errors detected. See MDIO register list and programming description for more information about at-speed BIST. BIST is disabled in Line or Special Line loopback modes.

IEEE 1149.1 (JTAG) and 1149.6 Operation

The SCAN12100 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at single-ended pins for interconnect testing. The TAP also provides access to the IEEE 1149.6 test features for differential pins. Refer to the (Boundary SCAN Description Language (BSDL) file located on National's website for the details of the IEEE1149.1 and 1149.6 implementation.

JTAG BIST and Enhanced BIST mode

The SCAN12100's at-speed BIST pattern generation and verification feature is normally accessed via the MDIO programming interface, however, the BIST can also be accessed through the JTAG bus. Access to the JTAG BIST command requires the SCAN12100 be run in local loopback BIST mode while RXCLK and ROUT[9:0] outputs are held in Tri-State. Under this mode, the device requires the REFCLKP/N input at 30.72MHz and runs PRWS10 pattern at 1.2288 Gbps.

In addition to this JTAG BIST, SCAN12100 can be re-programmed to operate in normal mode transceiver link mode, local loopback modes, all valid speed modes, all valid de-emphasis modes, and all valid equalization modes. To activate this advanced feature, a BSAMPLE instruction is executed. Then select data shift register and shift in the register of this order: {PE[1], PE[0], EQ[0], EQ[1], SPMODE[0], SPMODE[1], LOCAL_EN} On the TDI input, the generator will shift in a pattern that starts with LOCAL_EN and ends with PE[1]. For example, to set the device into 1.2288 Gbps with max EQ, max PE, and normal mode, shift from left to right 0, 1, 0, 1, 1, 1, and 1. SPMODE[1:0], PE[1:0], and EQ[1:0] follow the definitions in the datasheet except that MDIO will not override these parameters. The device default mode when SPMODE [1:0] = 2'b00 is 1.2288 Gbps. EQ[1:0] = 2'b00 and PE[1:0] = 2'b00 disable equalization and de-emphasis. Once the proper data has been shifted into the BSAMPLE data register, executing the JTAG BIST command places the device into BIST mode.

National recommends JTAG BIST run for at least 300ms to ensure BIST has been completed. Once 300ms has passed, the BIST result can be read through the data shift register. The output is mapped as follows: {BIST START, BIST COMPLETE, and BIST ERROR.} BIST START is shifted out first with BIST_ERROR last. If the test has been completed and passed, the shifted results will be 0, 1, and 1. If the BIST_START is 0, the receiver can not detect the BIST signal. If BIST_COMPLETE is 0, BIST run time is not long enough. If the BIST_ERROR goes 1, at least one bit error has occurred.

Instruction codes and device pin out are documented in the SCAN12100 BSDL file.

Precision Delay Calibration Measurement (DCM)

The SCAN12100 DCM circuitry delivers CPRI link and measurements, enabling the next generation distributed multi-hop base station architectures as well as advanced diversity, beam forming, and MIMO antenna systems. The DCM precisely measures absolute T14 and Toffset delays to better than ± 800 ps and can track delay changes (in fiber optics for example) with a resolution of 100's of picoseconds. Measurements are accessed via the MDIO interface as often as every 5 ms without interrupting CPRI link operation. The SCAN12100 not only reports accurate CPRI link and chip delays (chip latency is deterministic), but also enables measurement of intra-module RE timing such as TBdelays.

For more information about using DCM, ask your local National Semiconductor sales representative for the application note: "Precision Delay Calibration using National Semiconductor's SCAN25100."

MDIO Serial Control Interface

The MDIO serial control interface allows communication between a station management controller and SCAN12100 devices. MDIO and MDC pins are 3.3V LVTTL compliant, not 1.2V compatiable (see Electrical Characteristics table for detailed information). It is software compatible with the station management bus defined in IEEE 802.3ae-2002. The serial control interface consists of two pins, the data clock MDC and bidirectional data MDIO. MDC has a maximum clock rate of 2.5 MHz and no minimum limit. The MDIO is bidirectional and can be shared by up to 32 physical devices.

The MDIO pin requires a pull-up resistor which, during IDLE and turnaround, will pull MDIO high. The parallel equivalence of the MDIO when shared with other devices should not be less than 1.5 kΩ. Note that with many devices in parallel, the internal pull-up resistors add in parallel. Signal quality on the net should provide incident wave switching. It may be desirable to control the edge rate of MDC and MDIO from the station management controller to optimize signal quality depending upon the trace net and any resulting stub lengths.

In order to initialize the MDIO interface, the station management sends a sequence of 32 contiguous logic ones on MDIO with MDC clocking. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO high for 32 MDC clock cycles. A preamble is required for every operation (64-bit frames, do not suppress preambles).

MDC is an a periodic signal. Its high or low duration is 160 ns minimum and has no maximum limit. Its period is 400 ns minimum. MDC requires no timing or phase relationship to TXCLK, SYSCLK, or REFCLK. The following table shows the management frame structure in according to IEEE 802.3ae.

TABLE 15. 802.3ae MDIO Bus Protocol

Mgmt Bus Protocol	**<Preamble><Start><OpCode><PHY addr><dev addr><turnaround><data><idle>**
Address	<1…1><00><00><PPPPP><EEEEE><10><AAAA AAAA AAAA AAAA><idle>
Write	<1…1><00><01><PPPPP><EEEEE><10><DDDD DDDD DDDD DDDD><idle>
Read	<1…1><00><11><PPPPP><EEEEE><Z0><DDDD DDDD DDDD DDDD><idle>
Read-Increment-Address	<1…1><00><10><PPPPP><EEEEE><Z0><DDDD DDDD DDDD DDDD><idle>

<1…1> is a sequence of 32 contiguous ones and is used as preamble for synchronization purposes.

<PPPPP> is the PHY address of the device, defined by the logic states of ADD[4:0]. The MSB bit is the first bit transmitted or received. The PHY address is read at power-up or after a RESET event.

<EEEEE> is the device (register) address. The MSB bit is the first bit transmitted or received.

<AAAA AAAA AAAA AAAA> is the 16-bit address field of the register to be accessed. The first bit transmitted or received is bit 15.

<DDDD DDDD DDDD DDDD> is the 16-bit data field. It is the data to be written into the SCAN12100 when performing a Write operation. During the Read or Read-Increment-Address operation, it is the read-back data from the SCAN12100. The first bit transmitted or received is bit 15.

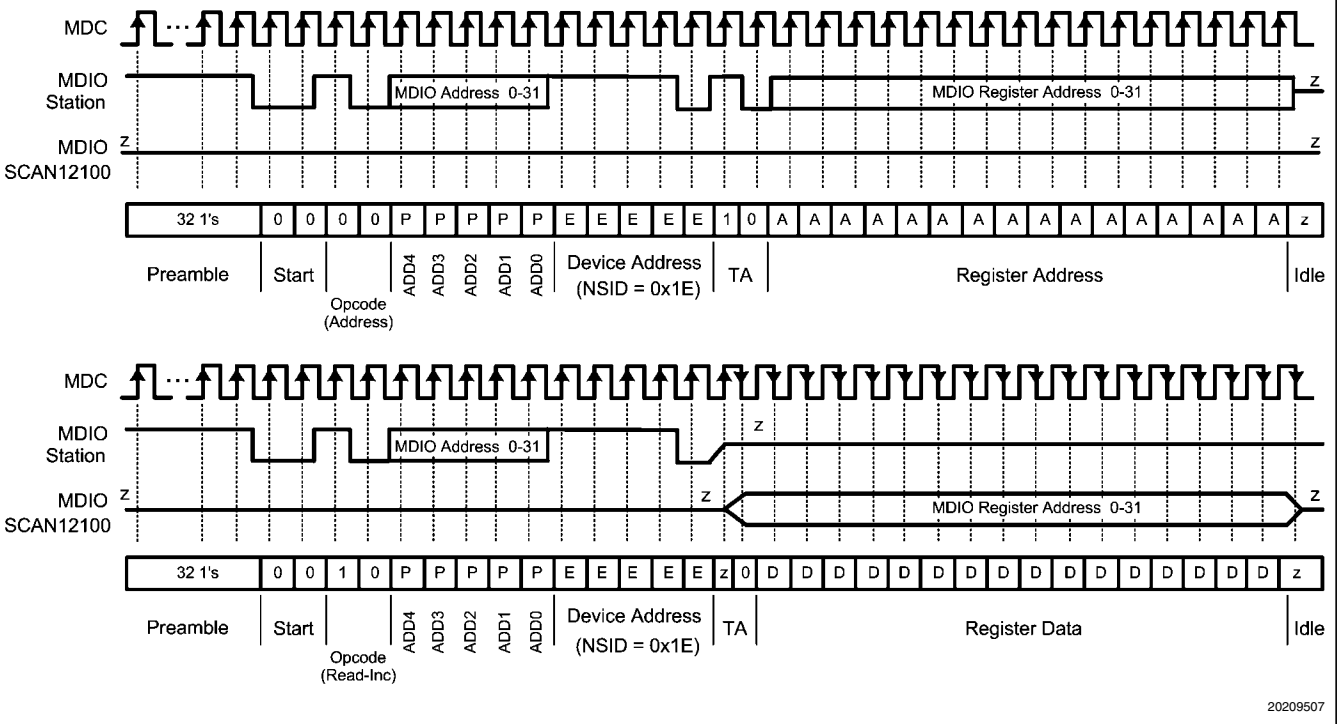
MDIO OPERATION

The MDIO interface is active when the SCAN12100 is powered up, REFCLK is present, and the SCAN12100 not being reset through the RESETB pin. The MDIO bus returns the following data:

- Correct PHY ADD, Correct DEV ADD — expected content
- Incorrect PHY ADD, Correct DEV ADD — FFFF'h
- Correct PHY ADD, Incorrect DEV ADD — 0000'h
- RESETB = Low — FFFF'h

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

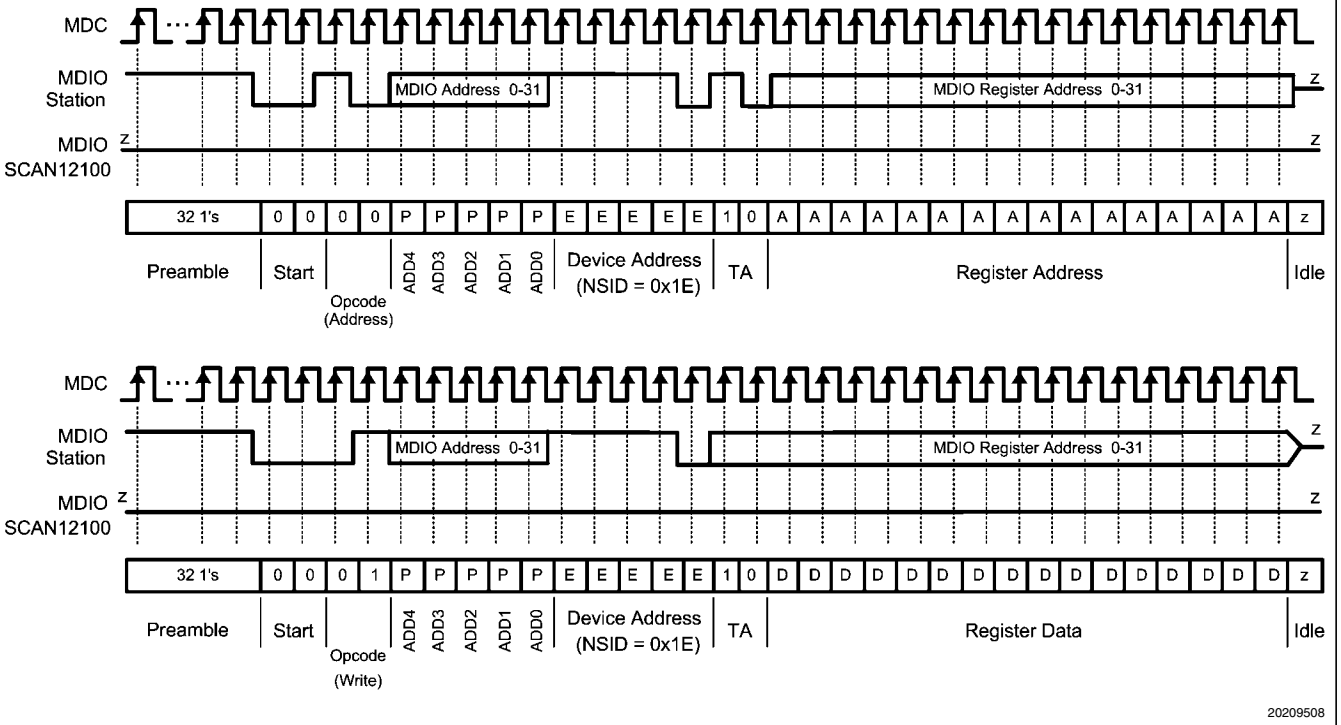
Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of the turnaround. The addressed SCAN12100 drives the MDIO with a zero for the second bit if the turnaround and follows this with the required data. *Figure 7* shows the timing relationship between MDC and MDIO as driven/received by the Station and the SCAN12100 for a typical read register access.



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FIGURE 7. Typical MDIO/MDC Read Operation

A normal write operation use the <01>. The data is latched in the SCAN12100 on each edge of the MDC clock. MDIO is sourced from the station side of the MDIO control interface.



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FIGURE 8. Typical MDIO/MDC Write Operation

Register Description

The SCAN12100 implements the device ID of 61 (0x3D.) Other registers defined by 802.3ae-2002 are not implemented in SCAN12100. The SCAN12100 has a rich MDIO register set to allow the chip to be controlled and monitored through software. Certain functions such as BIST and delay calibration are only accessible through MDIO.

The type of registers used in SCAN12100 are RW, RC, RO, and WC. RW is a read and write register. RC is a read and clear register. Upon reading the value of the RC register through MDIO, the register will reset its value. WC is a write and clear register. Write and clear registers are used for reset operations. A re-read of the WC register is necessary to verify the register has been cleared.

Address (hex)	Name	Access	Description
0	RESERVED	RW	Reserved.
1	POWERDOWN	RW	Transmiter and Receiver POWERDOWN control.
2	OUI	RO	OUI.
3	OUI Revision	RO	OUI, Device Product and Revision information.
4	RESET	RC	Transmiter and Receiver RESET control.
5	Rx Equalization	RW	CPRI LOF (Loss of Frame) bypass and Receiver EQ control.
6	Tx De-Emphasis	RW	Hyperframe size and Transmitter De-Emphasis control.
7	LOOPBACK	RW	Selects Normal, Line and Local Loopback.
8	MDIO	RO	Required by MDIO.
9	BIST	RW	Pattern and Enable control for Trasmit and Receive BIST.
A	Speed Mode	RW/Pin OW	Selects CPRI speed mode.
B	BIST Status	RC	BIST status information.
C	RESERVED	RO	Reserved.
D	DCM Start	RC	Initiates or restarts Delay Calibration Measurement.
E	OUI Duplicate	RO	Duplicate of Register Address 2.
F	OUI Rev. Duplicate	RO	Duplicate of Register Address 3.
10	LOF	RC	CPRI Loss of Frame (LOF) counter.
11	LOS	RC	CPRI Loss of Sync (LOS) counter.
12	Rx Lock	RC	Receiver Loss of Lock (LOCKB) counter.
13	Loss of Clock	RO	Loss of Transmit and/or Receive clock.
14	PLL Status	RO	Tx and Rx PLL status.
15	Hyperframe Length	RW	Programmable Hyperframe Length control.
16-17	DCM Trigger	RW	Delay Calibration Trigger pattern.
18	Reserved	RW	Reserved.
19	Hyperframe Tuning	RW	Programmable Hyperframe size and DCM enable
1A-1D	Reserved	RO	Reserved.
1E	T14 Lower	RO	T14 Measurement.
1F	T14 Upper	RO	T14 Measurement.
20	Toffset Lower	RO	Toffset Measurement.
21	Toffset Upper	RO	Toffset Measurement.
22	Tser Lower	RO	Tser Measurement.
23	Tser Upper	RO	Tser Measurement.
24	Tdes Lower	RO	Tdes Measurement.
25	Tdes Upper	RO	Tdes Measurement.
26	Tin-out Lower	RO	Tin-out Measurement.
27	Tin-out Upper	RO	Tin-out Measurement.
28	Tout-in Lower	RO	Tout-in Measurement.
29	Tout-in Upper	RO	Tout-in Measurement.

Note: The Default register values assume 614.4 mbps operation with the RESETB, RXCLKMODE, TXPWDN, and RXPWDN pins tied to a logic high.

4.1.0 Reserved

Address: 00h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Reserved	—	Reserved for future use. Returns undefined value when read.

4.1.1 Powerdown Control

Address: 01h Value: FFFFh

Bit	Default	Bit Name	Access	Bit Description
D15–D9	7'h7F	Reserved	—	Reserved for future use. Returns undefined value when read.
D8	1'b1	RX PWDNB	RW	**Receiver Powerdown:** Writing a [0] to this bit places the receiver of the SCAN12100 into a low power mode.
D7-D1	7'h7F	Reserved	—	Reserved for future use. Returns undefined value when read.
D0	1'b1	TX PWDNB	RW	**Transmiter Powerdown:** Writing a [0] to this bit places the transmiter of the SCAN12100 into a low power mode.

4.1.2 OUI

Address: 02h 0Eh Value: 2000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'h2000	OUI	RO	National Semiconductor identifier assigned by the IEEE.

4.1.3 OUI +

Address: 03h 0Fh Value: 5FD0h

Bit	Default	Bit Name	Access	Bit Description
D15-D10	6'h17	OUI[19:24]	RO	National Semiconductor identifier assigned by the IEEE.
D9-D4	6'h3D	Part Number	RO	SCAN12100 device identifier (3Dh).
D3-D0	4'h0	Revision	RO	SCAN12100 revision number.

4.1.4 Reset

Address: 04h Value: FFFFh

Bit	Default	Bit Name	Access	Bit Description
D15–D9	7'h7F	Reserved	—	Reserved for future use. Returns undefined value when read.
D8	1'b1	RX RESETB	WC	**Receiver Reset:** Writing [0] to this bit resets Rx control logic. Returns a value 1 after a few REFCLK cycles. If REFCLK is missing, the logic remains in reset mode.
D7-D1	7'h7F	Reserved	—	Reserved for future use. Undefined value returned when read.
D0	1'b1	TX PWDNB	WC	**Transmiter Reset:** Writing [0] to this bit resets Tx control logic. Returns a value 1 after a few REFCLK cycles. If REFCLK is missing, the logic remains in reset mode.

4.1.5 Receive Equalization

Address: 05h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15	1'b0	LOF Bypass	RW	Disables LOF control to allow DCM when using a non-CPRI hyperframe length
D14–D2	13'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D1-D0	2'd0	RX EQ	RW	**Receive Equalization:** Sets receive equalization when EQ[1:0] pins are low or floating.

4.1.6 Transmit De-Emphasis

Address: 06h Value: 2000h

Bit	Default	Bit Name	Access	Bit Description
D15–D8	8'h20	Hyperframe Size	RW	Sets non-CPRI hyperframe length
D7-D2	6'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D1-D0	2'b00	TX DE	RW	**Transmit De-Emphasis:** Sets transmit de-emphasis when PE[1:0] pins are low or floating.

4.1.7 Loopback Mode

Address: 07h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D4	12'h000	Reserved	RW	Reserved for future use. Returns undefined value when read.
D3-D0	4'b0000	Loopback	RW	Programs loopback mode
		4'b0000		Normal operation (no loopback)
		4'bxx10		Line loopback mode
		4'bxxx1		Local loopback mode
		4'b1000		Special local loopback mode
		4'b0100		Special line loopback mode
		4'b1100		Digital loopback mode
				All other combinations place device in normal operation.

4.1.8 MDIO

Address: 08h Value: 8000h

Bit	Default	Bit Name	Access	Bit Description
D15-D14	2'b10	Reserved	RO	Required MDIO bits. Returns 2'b10 when read.
D13-D0	14'd0	Reserved	—	Reserved for future use. Returns undefined value when read.

4.1.9 BIST Control

Address: 09h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15-D11	4'h0	Reserved	—	Reserved for future use. Returns undefined value when read.
D10	1'b0	RX Output Enable	RW	**Rx Output Enable:** Writing a [1] value enables ROUT pins in BIST mode.
D9-D8	2'b00	BIST Enable	RW	**[9] Rx BIST Verify, [8] Tx BIST Enable:** Writing 1's to these bits enables BIST mode. Tx and Rx BIST modes may be operated independently.
D7-D6	2'b00	Reserved	—	Reserved for future use. Returns undefined value when read.
D5-D4	2'b00	RX BIST	RW	Rx BIST Pattern Detect
		2b'00		CJPAT pattern (lane 0 per XAUI specification)
		2b'01		PRWS10 (Pseudo Random Word Sequence) pattern
		2b'10		Reserved pattern
		2b'11		CJPAT pattern (lane 0 per XAUI specification)
D3-D2	2'b00	Reserved	—	Reserved for future use. Returns undefined value when read.
D1-D0	2'b00	TX BIST	RW	Tx BIST Pattern Generation
		2b'00		CJPAT pattern (lane 0 per XAUI specification)
		2b'01		PRWS10 (Pseudo Random Word Sequence) pattern
		2b'10		Reserved pattern
		2b'11		CJPAT pattern (lane 0 per XAUI specification)

4.1.10 Speed Mode

Address: 0Ah Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D2	14'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D1-D0	2'd0	SPMODE	RW	Sets CPRI speed mode when SPMODE[1:0] pins are low or floating.

4.1.11 BIST Status

Address: 0Bh Value: 0100h

Bit	Default	Bit Name	Access	Bit Description
D15-D13	3'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D12	1'b1	BIST Stopped	RC	**BIST Stopped:** A value [1] will occur when Rx BIST verifier has been stopped.
D11	1'b0	BIST Error	RC	**BIST Error:** Returns a [1] value when the receive BIST verifier has been stopped or the BIST error count is greater than 10d'0. Returns a [0] value if no BIST errors.
D10	1'b0	BIST Detect	RC	Rx BIST verifier starts comparing the input data sequence after 3 cycles of properly aligned header sequences have been detected. A value of [1] implies that BIST verifier is checking the pattern. A read operation will **NOT** clear this bit nor will it reset the alignment of the pattern.
D9-D0	10'd0	Error Count	RC	This register displays the cumulative number of receive bit errors. The error count starts once a BIST pattern has been detected and the receive BIST verifier is enabled. This register counts a maximum of 10'h3FF errors and remains static as soon as BIST is stopped on the Rx verifier side. A read operation during the BIST enabled mode will **clear** the error count.

4.1.12 Reserved

Address: 0Ch Value: 0249h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'h0249	Reserved	RO	Reserved for future use. Returns undefined value when read.

4.1.13 Run DCM

Address: 0Dh Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D2	14'd0	Reserved	WC	Reserved for future use. Returns undefined value when read.
D1	1'b0	Reserved	WC	Reserved for future use. Returns undefined value when read.
D0	1'b0	Run DCM	WC	Writing a [1] runs DCM.

4.1.14 Loss of Frame (LOF)

Address: 10h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D9	7'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D8	1'd0	LOF Status	RC	CPRI loss of Frame (LOF) status. A [1] value indicates loss of CPRI frame. A [0] value indicates frame acquired.
D7-D0	8'h00	LOF Count	RC	Loss of frame count. The maximum count which can be accumulated in this register is 8'hFF.

4.1.15 Loss of Signal (LOS)

Address: 11h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D9	7'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D8	0'b0	LOS Status	RC	CPRI loss of signal (LOS) status. A value [1] indicates loss of frame.
D7-D0	8'd0	LOS Count	RC	Loss of signal count. The maximum count which can be accumulated in this register is 8'hFF.

4.1.16 Deserializer Loss of Lock

Address: 12h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D8	8'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D7-D0	8'd0	Loss of Rx Count	RC	Deserializer PLL loss of lock count since the last read operation of this register. The maximum count which can be accumulated in this register is 8'hFF. Note: During normal operation, receive PLL can go through multiple locking cycles before finally declaring lock. This is normal behavior.

4.1.17 Pin and Loss of Clock Status Registers

Address: 13h Value: 3015h

Bit	Default	Bit Name	Access	Bit Description
D15-D14	2'b00	SPMODE[1:0]	RO	SPMODE[1:0] pin status
D13	1'b1	TXPWDNB	RO	TXPWDNB pin status
D12	1'b1	RXPWDNB	RO	RXPWDNB pin status
D11	1'b0	Local Loopback	RO	A value [1] indicates local loopback is enabled
D10	1'b0	Line Loopback	RO	A value [1] indicates line loopback is enabled
D9	1'b0	Special Local Loopback	RO	A value [1] indicates special local loopback is enabled
D8	1'b0	Special Line Loopback	RO	A value [1] indicates special line loopback is enabled
D7	1'b0	Digital Loopback	RO	A value [1] indicates digital loopback is enabled
D6	1'b0	TX 10B mode	RO	
D5	1'b0	Rx 10B mode	RO	
D4	1'b1	RXCLKMODEB	RO	Inverted value of RXCLKMODE pin.
D3-D2	2'b01	Reserved	RO	Reserved for future use. Returns undefined value when read.
D1	1'b0	Loss of Tx Clock	RO	This register bit indicates a loss of TXCLK. A value of 1 indicates the TXCLK is not present or not running in the currently programmed speed mode.
D0	1'b1	Loss of Rx Clock	RO	This register bit indicates a loss of RXCLK. A value of 1 indicates the RXCLK is not present or not running in the currently programmed speed mode. The RXCLK feature is only supported in SCAN12100 READ mode operation.

4.1.18 Misc Status 2

Address: 14h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D8	8'd0	Reserved	—	Reserved for future use. Returns undefined value when read.
D7		RXCDR Lock - Ready	RO	A value [0] indicates the deserializer PLL is locked
D6-D2		Reserved	—	Reserved for future use. Returns undefined value when read.
D1		TXPLL Lock - Ready	RO	A value [1] indicates the serializer PLL is locked
D0		TXPLL Counter	RO	For internal use.

4.1.19 Start of Hyperframe Character

Address: 15h Value: 01BCh

Bit	Default	Bit Name	Access	Bit Description
D15-D10	6'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D9-D0	10'h1BC	8b Start of HF Character	RW	8b-bit mode start of hyperframe character

4.1.20 Start of Hyperframe Character

Address: 16h Value: 017Ch

Bit	Default	Bit Name	Access	Bit Description
D15-D10	6'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D9-D0	10'h17C	10b Start of HF Character+	RW	10b-bit mode start of hyperframe positive character

4.1.21 Start of Hyperframe Character

Address: 17h Value: 0283h

Bit	Default	Bit Name	Access	Bit Description
D15-D10	6'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D9-D0	10'h283	10b Start of HF Character-	RW	8b-bit mode start of hyperframe negative character

4.1.22 Reserved

Address: 18h Value: 0EF5h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'h0EF5	Reserved	—	Reserved for future use. Returns undefined value when read.

4.1.23 DCM

Address: 19h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15-D12	4'h0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D11	1'b0	Hyperframe Length Enable	RW	Enables non-standard CPRI length hyperframe to be used with DCM feature
D10-D9	2'b00	Initial Power up wait cycle	RW	These bits program the power up wait cycle for CPRI delay bias circuitry
		2'b00		66us
		2'b01		33us
		2'b10		66us
		2'b11		128us
D8-D1	7'd0	Reserved	RW	Reserved for future use. Returns undefined value when read.
D0	1'b0	Enable DCM	RW	A value [1] enables DCM control circuitry.

4.1.24 Reserved

Address: 1Ah 1Bh 1Ch 1Dh Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.

4.1.25 T14 Lower

Address 1Eh Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	T14 Lower	RO	Lower 16 T14 DCM bits. T14 is defined as Tx serial to Rx serial delay. This is the round trip delay of the cable + remote side.

4.1.26 T14 Upper

Address 1Fh Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D6	10'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	T14 Upper	RO	Upper 5 T14 DCM bits. T14 is defined as Tx serial to Rx serial delay. This is the round trip delay of the cable + remote side.

4.1.27 Toffset Lower

Address 20h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Toffset Lower	RO	Lower 16 Toffset DCM bits. Toffset is defined as the Rx serial to Tx serial delay.

4.1.28 Toffset Upper

Address 21h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D6	10'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	Toffset Upper	RO	Upper 5 Toffset DCM bits. Toffset is defined as the Rx serial to Tx serial delay.

4.1.29 Tser Lower

Address 22h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Tser Lower	RO	Lower 16 Tser DCM bits. Tser is defined as the serializer delay.

4.1.30 Tser Upper

Address 23h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D6	10'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	Tser Upper	RO	Upper 5 Tser DCM bits. Tser is defined as the serializer delay.

4.1.31 Tdes Lower

Address 24h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Tdes Lower	RO	Lower 16 Tdes DCM bits. Tdes is defined as the deserializer delay.

4.1.32 Tdes Upper

Address 25h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D6	10'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	Tdes Upper	RO	Upper 5 Tdes DCM bits. Tdes is defined as the deserializer delay.

4.1.33 Tin-out Lower

Address 26h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Tin-out Lower	RO	Lower 16 Tin-out DCM bits. Tin-out is defined as the delay between the Tx parallel inputs and the Rx parallel outputs.

4.1.34 Tin-out Upper

Address 27h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D6	10'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	Tin-out Upper	RO	Upper 5 Tin-out DCM bits. Tin-out is defined as the delay between the Tx parallel inputs and the Rx parallel outputs.

4.1.35 Tout-in Lower

Address 28h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D0	16'd0	Tout-in Lower	RO	Lower 16 Tout-in DCM bits. Tout-in is defined as the delay between the Rx parallel outputs and the Tx parallel inputs.

4.1.36 Tout-in Upper

Address 29h Value: 0000h

Bit	Default	Bit Name	Access	Bit Description
D15–D8	8'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D7	1'd0	DCM Error	RO	This bit is set to [1] if LOF is detected during DCM measurement
D6	1'd0	DCM Ready	RO	DCM results ready when this bit is [1]
D5	1'd0	Reserved	RO	Reserved for future use. Returns undefined value when read.
D4–D0	5'd0	Tout-in Upper	RO	Upper 5 Tout-in DCM bits. Tout-in is defined as the delay between the Rx parallel outputs and the Tx parallel inputs.

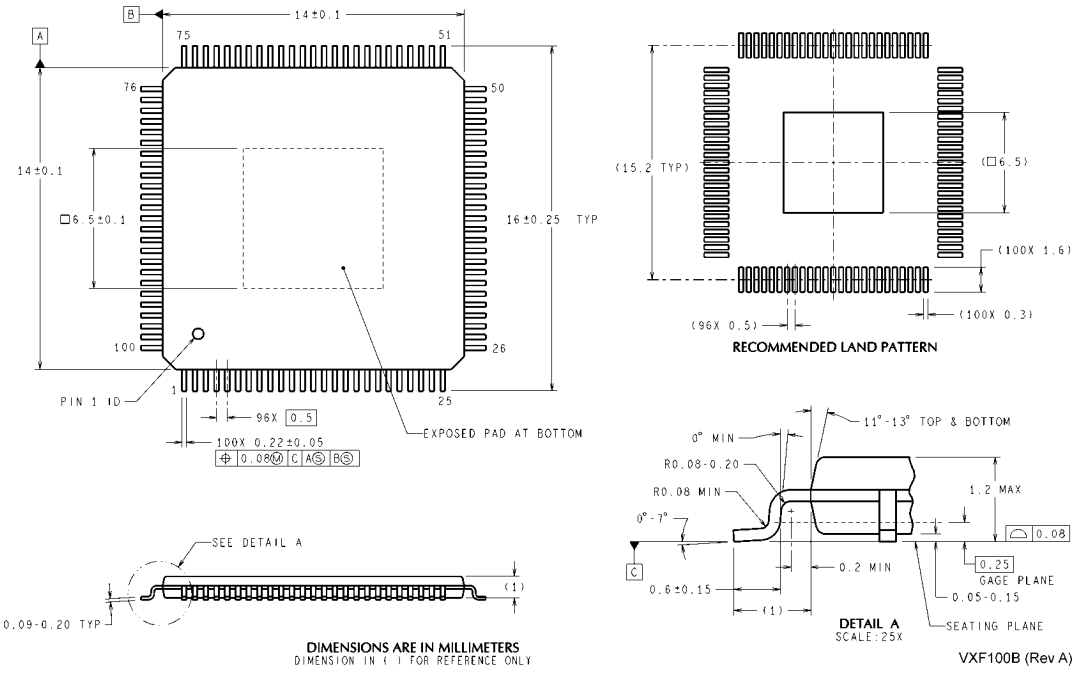
Design and Layout Guidelines

DESCRIPTION

The SCAN12100 is a 1228.8, and 614.4 Mbps serializer/deserializer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. This high-speed operation is achieved without significant layout and overall PCB design constraints. However, adhering to a few specific layout guidelines will optimize signal integrity and performance. The following list of topics is covered in National Semiconductor AN-1463.

1. AC coupling capacitor placement, size and value.
2. High speed differential signaling options (microstrip / stripline / twin-ax cable)
3. REFCLK terminations
4. DDR impedance recommendations
5. Decoupling
6. Power Filtering
7. Thermal recommendations

Physical Dimensions inches (millimeters) unless otherwise noted



100-Pin TQFP with Exposed Ground Pad (Top View)
Order Number SCAN12100TYA
NS Package Number VXF100B
See www.national.com/quality/marking_conventions.html for additional part marking information

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
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